Amendments to the Claims

The listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) An instruction fetch unit for a processor, comprising:

a first recoder to map an instruction from one encoded state to another encoded state; and

a second recoder to map an instruction from one encoded state to another encoded state, the second recoder coupled to the first recoder,

wherein the first recoder passes information regarding a first instruction belonging to a first instruction set architecture to the second recoder, and the second recoder recodes a second instruction belonging to the first instruction set architecture using the passed information to form a recoded instruction belonging to a second instruction set architecture.

2. (Original) The instruction fetch unit of claim 1, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

3. (Previously Presented) The instruction fetch unit of claim 1, wherein the processor executes instructions having X-bits and belonging to the first instruction set architecture and instructions having Y-bits and belonging to the second instruction set

architecture, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set architecture and the second instruction set architecture to form a recoded instruction having at least Y-bits.

4. (Previously Presented) The instruction fetch unit of claim 3, wherein each instruction of the first instruction set architecture has 16-bits and each instruction of the second instruction set architecture has 32-bits.

5. (Previously Presented) The instruction fetch unit of claim 3, wherein the first instruction set architecture includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set architecture, and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction.

6. (Original) The instruction fetch unit of claim 5, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction.

7. (Previously Presented) The instruction fetch unit of claim 3, wherein the first instruction set architecture includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits

to the second recoder thereby allowing the second recoder to recode the mode-switching instruction.

8. (Original) The instruction fetch unit of claim 7, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction.

9. (Currently Amended) A processor, comprising:

a first recoder to map an instruction from one encoded state to another encoded state; and

a second recoder to map an instruction from one encoded state to another encoded state, the second recoder coupled to the first recoder,

wherein the first recoder passes information regarding a first instruction belonging to a first instruction set architecture to the second recoder, and the second recoder recodes a second instruction belonging to the first instruction set architecture using the passed information to form a recoded instruction belonging to a second instruction set architecture.

10. (Original) The processor of claim 9, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

11. (Previously Presented) The processor of claim 10, wherein the processor executes instructions having X-bits and belonging to the first instruction set architecture and instructions having Y-bits and belonging to the second instruction set architecture, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set architecture and the second instruction set architecture to form a recoded instruction having at least Y-bits.

12. (Previously Presented) The processor of claim 11, wherein each instruction of the first instruction set architecture has 16-bits and each instruction of the second instruction set architecture has 32-bits.

13. (Previously Presented) The processor of claim 11, wherein the first instruction set architecture includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set architecture, and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction.

14. (Original) The processor of claim 13, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction.

15. (Previously Presented) The processor of claim 11, wherein the first instruction set architecture includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second

recoder thereby allowing the second recoder to recode the mode-switching instruction.

16. (Original) The processor of claim 15, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction.

17. (Currently Amended) A processing system, comprising:

a first recoder to map an instruction from one encoded state to another encoded state ~~for generating~~ that generates at least one information bit based on an expand instruction belonging to a first instruction set architecture; and

a second recoder~~, coupled to the first recoder, for recoding~~ that recodes an expandable instruction belonging to the first instruction set architecture using the at least one information bit generated to form a recoded instruction belonging to a second instruction set architecture.

18. (Original) The processing system of claim 17, further comprising:
an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

19. (Previously Presented) The processing system of claim 17, wherein the processing system executes instructions having X-bits and belonging to the first instruction set architecture and instructions having Y-bits and belonging to the second instruction set

architecture, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set architecture and the second instruction set architecture to form a recoded instruction having at least Y-bits.

20. (Previously Presented) The processing system of claim 19, wherein each instruction of the first instruction set architecture has 16-bits and each instruction of the second instruction set architecture has 32-bits.

21. (Previously Presented) The processing system of claim 19, wherein the expand instruction is used to enlarge an immediate field of the expandable instruction, and wherein the first recoder passes expand field bits to the second recoder.

22. (Previously Presented) The processing system of claim 21, wherein the expand field bits are concatenated to at least one bit of the expandable instruction.

23. (Currently Amended) A tangible computer readable storage medium comprising a microprocessor core embodied in software, the microprocessor core comprising:

a first recoder to map an instruction from one encoded state to another encoded state; and

a second recoder to map an instruction from one encoded state to another encoded state, the second recoder coupled to the first recoder,

wherein the first recoder passes information regarding a first instruction belonging to a first instruction set architecture to the second recoder, and the second recoder recodes a second instruction belonging to the first instruction set architecture using the passed information to form a recoded instruction belonging to a second instruction set architecture.

24. (Previously Presented) The tangible computer readable storage medium of claim 23, further comprising:

an instruction-staging unit coupled to the first recoder and the second recoder that dispatches an instruction from an instruction cache to one of the first recoder and the second recoder.

25. (Previously Presented) The tangible computer readable storage medium of claim 23, wherein the microprocessor core executes instructions having X-bits and belonging to the first instruction set architecture and instructions having Y-bits and belonging to the second instruction set architecture, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set architecture and the second instruction set architecture to form a recoded instruction having at least Y-bits.

26. (Previously Presented) The tangible computer readable storage medium of claim 25, wherein each instruction of the first instruction set architecture has 16-bits and each instruction of the second instruction set architecture has 32-bits.

27. (Previously Presented) The tangible computer readable storage medium of claim 25, wherein the first instruction set architecture includes an expand instruction used to enlarge an immediate field of an expandable instruction of the first instruction set architecture, and wherein the first recoder passes at least one bit of the expand instruction to the second recoder thereby allowing the second recoder to recode the expandable instruction.

28. (Previously Presented) The tangible computer readable storage medium of claim 27, wherein the at least one bit of the expand instruction is concatenated to at least one bit of the expandable instruction.

29. (Previously Presented) The tangible computer readable storage medium of claim 25, wherein the first instruction set architecture includes a mode-switching instruction that switches the operating mode of the processor, and wherein the first recoder passes one or more bits to the second recoder thereby allowing the second recoder to recode the mode-switching instruction.

30. (Previously Presented) The tangible computer readable storage medium of claim 29, wherein the one or more bits are concatenated to at least one bit of the mode-switching instruction.

31. (Previously Presented) A method for recoding instructions for execution by a processor, comprising:

(a) fetching an expand instruction belonging to a first instruction set architecture and an expandable instruction belonging to the first instruction set architecture;

(b) dispatching the expand instruction and the expandable instruction;

(c) generating at least one information bit based on the expand instruction; and

(d) recoding the expandable instruction using the at least one information bit generated to form a recoded instruction belonging to a second instruction set architecture.

32. (Previously Presented) The method of claim 31, wherein step (a) comprises:

(i) fetching the expand instruction during a first clock cycle of the processor; and

(ii) fetching the expandable instruction during a subsequent clock cycle of the processor.

33. (Previously Presented) The method of claim 31, wherein the at least one information bit based on the expand instruction is generated during a first clock cycle of the processor, and the expandable instruction is recoded during a second clock cycle of the processor.

34. (Previously Presented) The method of claim 33, further comprising a step between steps (c) and (d) of:

storing the at least one information bit in an information storage buffer.

35. (Currently Amended) A method for recoding instructions for execution by a processor, comprising:

fetching a plurality of instructions from an instruction cache, wherein the plurality of instructions includes a first instruction belonging to a first instruction set architecture and a second instruction belonging to the first instruction set architecture;

dispatching the first instruction to a first recoder that maps an instruction from one encoded state to another encoded state and the second instruction to a second recoder that maps an instruction from one encoded state to another encoded state; and

recoding the first instruction and the second instruction within a single clock cycle so as to form recoded instructions belonging to a second instruction set architecture for each of the first instruction and the second instruction.

36. (Previously Presented) The method of claim 35, wherein the recoding of the second instruction is performed using information from the first recoder.

37. (Previously Presented) The method of claim 35, further comprising forwarding at least one bit from the first recoder to the second recoder, wherein the at least one bit is used by the second recoder to perform a recoding operation.

38. (Currently Amended) An instruction fetch unit for a processor comprising:

a plurality of recoders that operate in parallel, each recoder mapping an instruction from one encoding state to another encoding state;

wherein the recoders recode instructions belonging to a first instruction set architecture within a single clock cycle so as to form recoded instructions belonging to a second instruction set.

39. (Previously Presented) The instruction fetch unit of claim 38, wherein one of the recoders recodes one instruction using information from another recoder.

40. (Previously Presented) The instruction fetch unit of claim 39, wherein the information includes at least one bit.

41. (Original) The instruction fetch unit of claim 1, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction.

42. (Original) The instruction fetch unit of claim 41, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field.

43. (Original) The processor of claim 9, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction.

44. (Previously Presented) The processor of claim 43, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field.

45. (Previously Presented) The tangible computer readable storage medium of claim 23, wherein the first instruction is used to enlarge a field of the second instruction and the information is at least one bit of the first instruction.

46. (Previously Presented) The tangible computer readable storage medium of claim 45, wherein the first instruction is an expand instruction, the second instruction is an expandable instruction and the field is an immediate field.